CLAIMS

1. A voltage/voltage converter for integrated circuits, the converter presenting a symmetrical multistage structure and comprising at least one input stage constituted by a clock booster circuit (CB) of symmetrical structure which delivers two output voltages, a voltage multiplier circuit of symmetrical structure comprising two voltage multiplier circuits (CM_i; CM_{ip}) respectively connected in two branches (B_1; B_2) of the converter and having the output voltages of the input stage applied respectively thereto, and an output stage (S) constituted by a multiplexer circuit (MX) having the two output voltages from the voltage multiplier stage applied thereto, the converter being characterized in that each voltage multiplier circuit (CM_i; CM_{ip}) is controlled by a control circuit (CC_i; CC_{ip}), and in that each voltage multiplier circuit (CM_i; CM_{ip}) supplies voltages needed both for the operation of its own control circuit and for the operation of the control circuit of the other voltage multiplier circuit of the same stage.

2. A converter according to claim 1, characterized in that the clock booster circuit (CB) serves to add a DC component to a clock signal, and in that the clock booster circuit (CB) comprises two similar circuits receiving respective clock signals (ϕ_1; ϕ_2) of opposite phase.

3. A converter according to claim 1 or claim 2, characterized in that each voltage multiplier circuit (CM_i; CM_{ip}) comprises a capacitor (C_i; C_{ip}) and a switch (K_i; K_{ip}) for controlling charging of the capacitor and transfer of its charge to the voltage multiplier circuit of the following stage.

4. A converter according to any preceding claim, characterized in that it has a positive output, in that

the clock booster circuit (CB) forming the input stage has a positive output and comprises two NMOS transistors and two capacitors, in that the drain of each transistor (M_1; M_{1p}) is connected to a power supply terminal (V_{dd}), the source of each transistor (M_1; M_{1p}) is connected to the positive electrode of the capacitor (C_1; C_{1p}) of the associated branch, and the grid of each transistor (M_1; M_{1p}) is connected to the positive electrode of the capacitor (C_1; C_{1p}) and to the source of the transistor in the opposite branch, and in that the negative electrodes of the capacitors (C_1; C_{1p}) are respectively connected to two clock signals (ϕ_1; ϕ_2) in phase opposition.

5. A converter according to claim 3 or claim 4, characterized in that the capacitors (C_i; C_{ip}) of the two branches (B_1; B_2) of the voltage multiplier stage have their positive electrodes respectively connected to the outputs of two switches (K_i; K_{ip}) via two nodes (V_i; V_{ip}), and their negative electrodes connected to respective clock signals (ϕ_i), in that an input of each switch (K_i; K_{ip}) is connected to the output of the preceding stage, and in that the clock signal (ϕ_i) corresponds either to the signal (ϕ_1) if $\underline{i}$ is odd for the first branch (B_1) and to the signal (ϕ_2) if $\underline{i}$ is even for the first branch (B_1), or to the signal (ϕ_2) if $\underline{i}$ is odd for the second branch (B_2) and to (ϕ_1) if $\underline{i}$ is even for the second branch (B_2).

6. A converter according to any preceding claim, characterized in that the control circuit (CC_i) of the voltage multiplier circuit (CM_i) of the first branch (B_1) is an inverter circuit (I_i) which is powered between the voltage (V_{i-1}) from the voltage multiplier circuit of the preceding stage in the first branch (B_1), and the voltage (V_{ip}) from the voltage multiplier circuit of the same stage in the second branch (B_2), and in that the inverter (I_i) is controlled either by the voltage ($V_{c(i-1)}$) of the preceding voltage multiplier circuit of the first branch

(B_1) or by the voltage (V_i) from the voltage multiplier circuit (CM_i) of the first branch (B_1).

7. A converter according to any preceding claim, characterized in that the control circuit (CC_{ip}) of the voltage multiplier circuit (CM_{ip}) of the second branch (B_2) is an inverter circuit (I_{ip}) which is powered between the output voltage ($V_{(i-1)p}$) of the voltage multiplier circuit ($CM_{(i-1)p}$) of the preceding stage of the second branch (B_2) and the output voltage (V_i) of the voltage multiplier circuit (CM_i) of the same stage of the first branch (B_1), and in that the inverter (I_{ip}) is controlled either by the output voltage ($V_{c(i-1)p}$) of the preceding voltage multiplier circuit of the second branch (B_2) or by the voltage (V_{ip}) of the voltage multiplier circuit (CM_{ip}) of the second branch (B_2).

8. A converter according to any preceding claim, characterized in that the voltage circuit (MX) recovers the highest voltages from the voltage multiplier circuits (CM_i; CM_{ip}) and, by switching, extracts therefrom the highest DC voltage forming the output voltage of the converter.

9. A converter according to claim 8, characterized in that the multiplexer circuit (MX) has a positive output and comprises two switches (K_{s1}; K_{s2}) connected to the output terminal (V_s) of the multiplexer circuit and to the output terminals (V_{Np}; V_N) of the voltage multiplier stage (N-1), in that the two switches (K_{s1}; K_{s2}) are controlled by the output signals from two inverter circuits ($I_{(N+1)p}$; I_{N+1}), and in that the multiplexer circuit also comprises an auxiliary circuit having the function of generating the control signals for the switches (K_{s1}; K_{s2}).

10. A converter according to claim 9, characterized in that the auxiliary circuit comprises two inverters

($I_{(N+1)p}$; I_{N+1}), two switch circuits (K_{s3}; K_{s4}), and two capacitors ($C_{(N+1)p}$; C_{N+1}).

11. A converter according to claim 10, characterized in that the two switches (K_{s3}; K_{s4}) share the same control signal and the same input signal as the two switches (K_{s1}; K_{s2}), in that the switch (K_{s3}) is connected between the output voltage (V_{Np}) and the positive electrode of the converter ($C_{(N+1)p}$) whose negative electrode is connected to the clock signal ($\phi_{(n+1)p}$), in that the switch (K_{s4}) is connected between the output voltage (V_N) of the multiplier circuit (CM_N) of the first branch (B_1) of the stage N of the converter at the positive electrode of the capacitor (C_{N+1}) whose negative electrode is connected to the clock signal (ϕ_{n+1}), and in that the two inverters ($I_{(N+1)p}$; I_{N+1}) have respective input signals (V_{cNp}; V_{cN}) and are respectively powered between the voltages (V_{Np}; V_N) as their low power supply voltages and (V_{N+1}; $V_{(n+1)p}$) as their high power supply voltages.

12. A converter according to claim 10, characterized in that the two switches (K_{s3}; K_{s4}) have the same control signal and the same input signal as the two switches (K_{s1}; K_{s2}), in that the switch (K_{s3}) is connected between the output voltage (V_{Np}) and the positive electrode of the capacitor ($C_{(N+1)p}$) whose negative electrode is connected to the clock signal ($\phi_{(n+1)p}$), in that the switch (K_{s4}) is connected between the output voltage (V_N) of the multiplier circuit (CM_N) and the first branch (B_1) of the stage N of the converter and the positive electrode of the capacitor (C_{N+1}) whose negative electrode is connected to the clock signal (ϕ_{n+1}), and it that the two inverters ($I_{(N+1)p}$; I_{N+1}) have as their respective input signals ($V_{(N+1)p}$; V_{N+1}) and are respectively powered between the voltages (V_{Np}; V_N) as their low power supply voltages and (V_{N+1}; $V_{(N+1)p}$) as their high power supply voltages.

13. A converter according to any one of claims 1 to 3, characterized in that its output is negative, in that the clock booster circuit forming the input stage has a negative output and comprises two PMOS transistors and two capacitors, in that the drain of each transistor (M_1; M_{1p}) is connected to ground, the source of each transistor (M_1; M_{1p}) is connected to the negative electrode of the capacitor (C_1; C_{1p}) of the associated branch, and the grid of each transistor (M_1; M_{1p}) is connected to the positive electrode of the capacitor (C_1; C_{1p}) and to the source of the transistor of the opposite branch, and in that the positive electrodes of the capacitors (C_1; C_{1p}) are respectively connected to two clock signals (ϕ_1; ϕ_2) in phase opposition.

14. A converter according to claim 13, characterized in that the capacitors (C_i; C_{ip}) of the two branches (B_1; B_2) of the voltage multiplier stage have their positive electrodes respectively connected to the outputs of two switches (K_i; K_{ip}) via two nodes (V_i; V_{ip}), and their negative electrodes connected to respective clock signals (ϕ_i), in that an input of each switch (K_i; K_{ip}) is connected to the output of the preceding stage, and in that the clock signal (ϕ_i) corresponds either to the signal (ϕ_1) if $\underline{i}$ is odd for the first branch (B_1) and to the signal (ϕ_2) if $\underline{i}$ is even for the first branch (B_1), or to the signal (ϕ_2) if $\underline{i}$ is odd for the second branch (B_2) and to (ϕ_1) if $\underline{i}$ is even for the second branch (B_2).

15. A converter according to claim 13 or claim 14, characterized in that the control circuit (CC_i) of the voltage multiplier circuit (CM_i) of the first branch (B_1) is an inverter circuit (I_i) which is powered between the voltage (V_{i-1}) from the voltage multiplier circuit of the preceding stage in the first branch (B_1), and the voltage (V_{ip}) from the voltage multiplier circuit of the same stage in the second branch (B_2), and in that the inverter

(I_i) is controlled either by the voltage ($V_{c(i-1)}$) of the preceding voltage multiplier circuit of the first branch (B_i) or by the voltage (V_i) from the voltage multiplier circuit (CM_i) of the first branch (B_1).

16. A converter according to any one of claims 13 to 15, characterized in that the control circuit (CC_{ip}) of the voltage multiplier circuit (CM_{ip}) of the second branch (B_2) is an inverter circuit (I_{ip}) which is powered between the output voltage ($V_{(i-1)p}$) of the voltage multiplier circuit ($CM_{(i-1)p}$) of the preceding stage of the second branch (B_2) and the output voltage (V_i) of the voltage multiplier circuit (CM_i) of the same stage of the first branch (B_1), and in that the inverter (I_{ip}) is controlled either by the output voltage ($V_{c(i-1)p}$) of the preceding voltage multiplier circuit of the second branch (B_2) or by the voltage (V_{ip}) of the voltage multiplier circuit (CM_{ip}) of the second branch (B_2).

17. A converter according to any one of claims 13 to 16, characterized in that the voltage circuit (MX) recovers the highest voltages from the voltage multiplier circuits (CM_i; CM_{ip}) and, by switching, extracts therefrom the highest DC voltage forming the output voltage of the converter.

18. A converter according to claim 17, characterized in that the multiplexer circuit (MX) has a positive output and comprises two switches (K_{s1}; K_{s2}) connected to the output terminal (V_s) of the multiplexer circuit and to the output terminals (V_{Np}; V_N) of the voltage multiplier stage (N-1), in that the two switches (K_{s1}; K_{s2}) are controlled by the output signals from two inverter circuits ($I_{(N+1)p}$; I_{N+1}), and in that the multiplexer circuit also comprises an auxiliary circuit having the function of generating the control signals for the switches (K_{s1}; K_{s2}).

19. A converter according to claim 18, characterized in that the auxiliary circuit comprises two inverters ($I_{(N+1)p}$; I_{N+1}), two switch circuits (K_{s3}; K_{s4}), and two capacitors ($C_{(N+1)p}$; C_{N+1}).

20. A converter according to claim 19, characterized in that the two switches (K_{s3}; K_{s4}) share the same control signal and the same input signal as the two switches (K_{s1}; K_{s2}), in that the switch (K_{s3}) is connected between the output voltage (V_{Np}) and the positive electrode of the converter ($C_{(N+1)p}$) whose negative electrode is connected to the clock signal ($\phi_{(n+1)p}$), in that the switch (K_{s4}) is connected between the output voltage (V_N) of the multiplier circuit (CM_N) of the first branch (B_1) of the stage N of the converter at the positive electrode of the capacitor (C_{N+1}) whose negative electrode is connected to the clock signal (ϕ_{n+1}), and in that the two inverters ($I_{(N+1)p}$; I_{N+1}) have respective input signals (V_{cNp}; V_{cN}) and are respectively powered between the voltages (V_{Np}; V_N) as their low power supply voltages and (V_{N+1}; $V_{(n+1)p}$) as their high power supply voltages.

21. A converter according to claim 19, characterized in that the two switches (K_{s3}; K_{s4}) have the same control signal and the same input signal as the two switches (K_{s1}; K_{s2}), in that the switch (K_{s3}) is connected between the output voltage (V_{Np}) and the positive electrode of the capacitor ($C_{(N+1)p}$) whose negative electrode is connected to the clock signal ($\phi_{(n+1)p}$), in that the switch (K_{s4}) is connected between the output voltage (V_N) of the multiplier circuit (CM_N) and the first branch (B_1) of the stage N of the converter and the positive electrode of the capacitor (C_{N+1}) whose negative electrode is connected to the clock signal (ϕ_{n+1}), and it that the two inverters ($I_{(N+1)p}$; I_{N+1}) have as their respective input signals ($V_{(N+1)p}$; V_{N+1}) and are respectively powered between the

voltages (V_{Np}; V_N) as their low power supply voltages and (V_{N+1}; $V_{(N+1)p}$) as their high power supply voltages.